

Open Graphics Project

Product Specification

This document describes a preliminary feature set for the Tech Source Open Graphics card. It is being published as a status update and as a call for more feedback from the community so that we can identify any important features which may be missing. There are no guarantees that any listed features will appear in the final product.

Target audience

This open graphics product is targeted primarily at open source desktop users. While there will be enough 3D capability to support many complex 3D games, the design is not optimized for games. The primary motivation for supporting 3D graphics is because the latest GUIs have started to require 3D features.

Physical component break-down

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| PCB | <ul style="list-style-type: none">• half-height/half-length PCI, AGP, and PCI-Express versions |
| GPU | Reprogrammable Xilinx Spartan III 2000 FPGA |
| ROMs | <ul style="list-style-type: none">• BIOS/firmware• Serial prom for FPGA |
| RAM | 128 Megabytes (four 256 megabit chips) |
| Video | DVI-I providing digital and analog, pin header and expansion kit for TV out |
| Host interface | PCI, AGP, then PCI-Express |
| Misc. | DVI-I connector, face plate, power supply, general (user) I/O header |

GPU component break-down

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| Host interface | <ul style="list-style-type: none">• PCI and AGP 4x versions, PCI-Express• DMA for rendering commands• YUV<->RGB conversion• Emulation of 8-bit and 16-bit pixel formats• Bit swapping for big-endian/little-endian conversion• Some MesaGL security features (possible feature)• Interrupts for rendering and DMA state changes• Other features: Logic ops, planemasks |
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| Video | <ul style="list-style-type: none"> • Single channel (multi-channel in future) • Fully programmable, supporting VESA, DVI reduced-blanking, progressive scan, interlaced, etc. • Up to 250Mhz (165Mhz for DVI) pixel clock • Single 64x64 full-color alpha-blended hardware cursor • Integer scaling (possible feature) • Window-ID, 8-bit overlay, dual-LUT • Vertical interrupts • TV out (S-Video, component YUV, NTSC, PAL, SECAM) • DDC/EDID |
| Memory | <ul style="list-style-type: none"> • Quad-channel 400Mhz DDR • Maximum total bandwidth: 1.6 billion pixels/second • Linear and tiled addressing • DMA bypass for accessing host images |
| VGA | <ul style="list-style-type: none"> • 80x25 text, 640x480x16, etc. • Can be disabled for secondary cards |
| 3D renderer | <ul style="list-style-type: none"> • Supports most of OpenGL 1.3, plus some later features • Extensions for 2D (see below) |
| Misc. | PROM reading/writing interface, peripheral bus, user-programmable I/O |

Rendering engine features

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| Data format | <ul style="list-style-type: none"> • All rendering coordinates and color components are 25-bit float. • Framebuffer pixels are always 32-bit ARGB. |
| Performance | <ul style="list-style-type: none"> • Dual-pixel pipeline at 200 Mhz • 400 million pixels/second [*] • Triangle rate limited by host interface speed |
| Gouraud shading | <ul style="list-style-type: none"> • Linear stepping with perspective correction • Diffuse and specular |
| Texture mapping | <ul style="list-style-type: none"> • Linear stepping over 1D/2D textures, with perspective correction • Bilinear interpolation • Arbitrary-size non-repeated textures • Power-of-two sized repeated textures • MIPmaps and Trilinear interpolation • Two texture units |
| Other 3D features | <ul style="list-style-type: none"> • Depth buffering (25-bit float W-buffering) • Fog • Ownership, Alpha, and Scissor tests • Alpha blend • Arithmetic raster-op • Stencil test |

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| 2D features | <ul style="list-style-type: none">• Polylines (solid and patterned) [**]• Plane mask• Logical raster-op (GDI ROP4)• Patterns (8x8 color, 32x32 mono)• Rectangular clipping• Color key and mask |
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Open Source software

- Linux drivers (DRI, X.org, MesaGL) under BSD+MIT+GPL licenses
- Windows drivers (if possible, considering IP constraints)
- x86 PC BIOS
- Sun OpenBoot

NOTES

[*] Different parts of the pipeline attempt to access memory simultaneously. There is a total bandwidth limit of 1.6 billion pixels/second. This means that although a bitblt/texture operation doubles the memory bandwidth requirement as compared to as solid fill (read 400MP/s and write 400MP/s, for a total of 800MP/s), the pipeline will still operate at full speed because the limit of 1600MP/sec hasn't been reached.

[**] Having a unified pipeline, most 2D rendering primitives are drawn as special cases of 3D primitives.